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SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)

B.Tech III Year II Semester Regular & Supplementary Examinations October-2020
COMPILER DESIGN

(Common to CSE & CSIT)

Time: 3 hours

Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

- 1 a Illustrate the step by step process to design the compiler by using the source program **8M**
position: =initial + rate * 60
b Write the applications of compiler technology **4M**
OR
- 2 a Write the Role of a Lexical Analysis phase and Explain LEX Tool with a Lex Programme. **8M**
b What is pass and phases of a compiler? Explain. **4M**

UNIT-II

- 3 a Calculate FIRST and FOLLOW for the following grammar. **8M**
E-> E+T/T
T-> T*F/F
F-> (E)/id
b Write the differences between SLR, CLR, LALR parsers. **4M**
OR
- 4 Construct CLR Parsing table for the given grammar **12M**
S->CC
C->aC/d

UNIT-III

- 5 a List and Explain the applications of Syntax Directed Definition. **6M**
b Describe the evaluation order of SDT with an example. **6M**
OR
- 6 a Explain the Type Checking with suitable examples. **5M**
b What is Backpatching? Explain in detail about Back patching Technique. **7M**

UNIT-IV

- 7 What is Activation Record? Draw the format of Activation Record in stack allocation and explain each field in it. **12M**
OR
- 8 Distinguish between static scope and dynamic scope. Briefly explain access to non-local Names in static scope. **12M**

UNIT-V

- 9 Illustrate the various strategies in register allocation. **12M**
OR
- 10 Explain the peephole optimization Technique with example. **12M**

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